

Appl. No. 10/749,910
Amdt. dated March 9, 2006
Reply to Office Action of December 19, 2005

PATENT

REMARKS/ARGUMENTS

This Amendment is in response to the Office Action mailed December 19, 2005. Claims 1-13 were pending in the present application. The present response amends claims 1-2, 7-8, and 13; cancels claim 4; and adds new claims 14-17, leaving pending in the application claims 1-3 and 5-17. Reconsideration of the rejected claims and consideration of the newly presented claims is respectfully requested.

I. Rejection under 35 U.S.C. §112

Claim 4 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants respectfully submit that claim 4 has been canceled, such that the rejection is now moot.

II. Rejection under 35 U.S.C. §103

(a) Bronson and Schulz

Claims 1-4, 6-10, and 12-13 are rejected under 35 U.S.C. §103(a) as being obvious over *Bronson* (US 6,279,064) in view of *Schulz* (US 6,959,374). Applicants respectfully submit that *Bronson* and *Schulz* fail to teach or suggest all elements recited in these claims.

For example, Applicants' claim 1 as amended recites a memory controller, comprising:

- at least one bus interface, each bus interface being for connection to at least one respective device for receiving memory access requests;
- a memory interface, for connection to a memory device over a memory bus;
- a plurality of buffers; and
- control logic, for placing received memory access requests into a queue of memory access requests,
 - wherein, in response to a received memory access request requiring multiple data bursts over the memory bus, data from each of said multiple data bursts is stored in a respective buffer of said plurality of buffers, and
 - wherein, for a wrapping memory access request requiring multiple buffers, data required for a beginning and an end of the wrapping memory access request are stored in a single buffer of the plurality of buffers

(*emphasis added*). Such elements are neither taught nor suggested by these references.

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Bronson teaches a queuing system in an I/O bus bridge that processes interrupt commands and controls the discrete interrupt lines to individual processors (col. 3, lines 26-35). As recognized in the Office Action, *Bronson* does not teach or suggest a memory controller wherein "in response to a received memory access request requiring multiple data bursts over the memory bus, data from each of said multiple data bursts is stored in a respective buffer of said plurality of buffers" (OA p. 3). *Bronson* also fails to teach or suggest, "for a wrapping memory access request requiring multiple buffers, data required for a beginning and an end of the wrapping memory access request are stored in a single buffer of the plurality of buffers" as recited in Applicants' claim 1. As such, claim 1 cannot be rendered obvious by *Bronson*.

Schulz does not make up for this deficiency in *Bronson* with respect to claim 1. *Schulz* teaches data "pre-fetching," wherein a number of read cycles are performed "to a number of sequential addresses in memory," each of these sequential cache lines of data then being stored in cache memory (col. 1, line 65-col. 2, line5). Each cache line can be stored in a storage buffer (col. 4, lines 48-52). *Schulz* does not teach or suggest handling a wrapping data request, but instead is directed to a pre-fetching of subsequent data that might be requested in subsequent requests. Further, *Schulz* does not teach or suggest, "for a wrapping memory access request requiring multiple buffers, data required for a beginning and an end of the wrapping memory access request are stored in a single buffer of the plurality of buffers" as recited in Applicants' claim 1. As such, claim 1, and dependent claims 2-3, 6, and 14-15, cannot be rendered obvious by *Schulz*, either alone or in combination with *Bronson*. Independent claims 7 and 13, and dependent claims 8-10, 12, and 16-17, recite similar limitations that also are not rendered obvious by *Bronson* and *Schulz*. As such, Applicants respectfully request that the rejection with respect to claims 1-3, 6-10, and 12-13 be withdrawn.

(b) *Bronson, Schulz, and Secatch*

Claims 5 and 11 are rejected under 35 U.S.C. §103(a) as being obvious over *Bronson* and *Schulz* in view of *Secatch* (US 2003/0131162). Claims 5 and 11 depend from claims 1 and 7, respectively, which are not rendered obvious by *Bronson* and *Schulz* as discussed above. *Secatch* does not make up for the deficiencies in these references with respect to these claims.

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Secatch teaches a non-destructive read FIFO queue, which allows data read from an address in the queue to be re-read from the same address in the queue in a subsequent read cycle (paragraph [0007]). *Secatch* does not, however, teach or suggest, "for a wrapping memory access request requiring multiple buffers, data required for a beginning and an end of the wrapping memory access request are stored in a single buffer of the plurality of buffers" as recited in Applicants' claim 1, or similarly in Applicants' claim 7. As such, claims 1 and 7, as well as dependent claims 5 and 11, cannot be rendered obvious by *Secatch*, either alone or in combination with *Bronson* and/or *Schulz*. Applicants therefore respectfully request that the rejection with respect to claims 5 and 11 be withdrawn.

III. Amendment to the Claims

Unless otherwise specified, amendments to the claims are made for purposes of clarity, and are not intended to alter the scope of the claims or limit any equivalents thereof. The amendments are supported by the specification and do not add new matter.

IV. Newly Presented Claims

Claims 14-17 have been added to cover different aspects of the present invention. These claims are supported by the specification and do not add new matter. Applicants therefore respectfully request consideration of newly presented claims 14-17.

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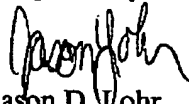
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CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,


Jason D. Lohr
Reg. No. 48,163

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
Attachments
JDL:asb
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